REMARKS/ARGUMENTS

Claims 1-30 stand rejected in the outstanding Official Action. Claims 1-8 and 16-23 have been cancelled without prejudice and claims 9 and 24 amended. Accordingly, claims 9-15 and 24-30 are the only claims remaining in this application.

The Examiner indicates that the title is not descriptive of the claimed invention. Applicant has amended the title to read "PREFETCHING EXCEPTION VECTORS BY EARLY LOOKUP OF EXCEPTION VECTORS WITHIN A CACHE MEMORY" which is believed to be more descriptive of the claimed invention. However, should the Examiner have a more concrete suggestion, Applicant will certainly consider any proposal.

Claims 1-6, 9-13, 16-21 and 24-28 stand rejected under 35 USC §102 as anticipated by Nguyen (U.S. Patent 5,481,685). While Applicant has cancelled claims 1-8 and 16-23, independent apparatus and method claims 9 and 24, respectively, have been amended to specify the structure of an instruction pipeline including an instruction prefetch unit and the method step of processing program instructions with an instruction pipeline including an instruction prefetch unit.

Specifically, Applicant's apparatus and method claims require the structure of "an exception controller" (claim 9) and a "triggering" step (claim 24) in which, where the exception signal is received partway through execution of a current program, the exception controller triggers a lookup of an exception handling program instruction within the cache memory and if not included within the cache memory, triggers a cache line fill operation to read the exception handling program instruction from a main memory to a cache memory. If the current program instruction has been completed and if the exception is still current, the instruction prefetch unit

fetches the exception handling program instruction from the cache memory. Therefore, in order to anticipate Applicant's combination of a cache memory, an instruction pipeline and a particular exception controller, it is necessary that the Nguyen reference teach all three structures and teach those structures combined in the manner of Applicant's independent claims 9 and 24.

The Nguyen reference initiates prefetching of an exception as soon as it is seen by the virtual memory unit (VMU) ("[i]n both cases, the PC logic unit handles the error condition by storing the current execution point in the instruction stream and then prefetching, as if in response to an unconditional branch, a dedicated exception handling routine instruction stream for diagnosing and handling the error condition" – column 12, lines 47-52). The Nguyen reference will result in clock cycle delay while the prefetching is processed by the virtual memory unit and then the program counter logic unit will generate the prefetch address. The prefetch instructions are then placed in one of three prefetch buffers. These are clear clock cycle delays which are taught by the Nguyen reference.

There is no disclosure or suggestion in Nguyen of any early triggering of a cache lookup, and possible cache linefill within the cache memory accompanied by a deferral of fetching the exception handling program instructions by the prefetch unit until the instruction boundary has actually been reached. As a result, Applicant does not believe that Nguyen teaches the structures and method steps recited in Applicant's independent claims 9 and 24, respectively, and the Examiner is respectfully requested to point out how or where he sees each of the claimed elements or method steps in the Nguyen '685 reference.

Claims 7, 8, 14, 15, 22, 23, 29 and 30 stand rejected under 35 USC §103 as unpatentable over Nguyen in view of Glass (U.S. Patent 5,784,602). The Examiner's admission that Nguyen

"fails to disclose a common core for processor components or, more generally, an integrated circuit" is very much appreciated.

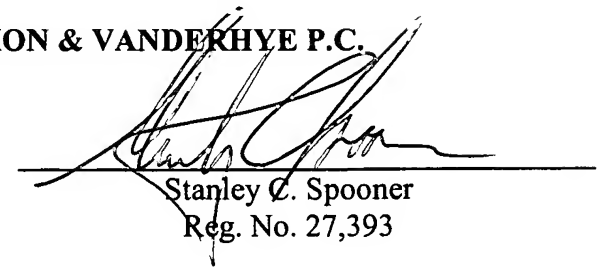
The Glass reference is cited for teaching a system on an integrated circuit. However, there is no disclosure in Glass, nor does the Examiner even allege that Glass, discloses the "exception controller" as set out in Applicant's independent claim 9 or the "triggering" step set out in Applicant's independent claim 24. These are features positively recited in Applicant's two independent claims which are not present in either the Nguyen or Glass references. Therefore, without any disclosure of these claimed structural elements and method steps, the two references, even when combined, cannot disclose or render obvious the claimed invention.

Additionally, the Examiner's conclusory statement that it would have been obvious to combine the references does not meet the test of the Court of Appeals for the Federal Circuit of demonstrating some "reason" or "motivation" for combining references. As a result, there is no *prima facie* basis of rejection for remaining claims 14, 15, 29 and 30 and any further rejection under 35 USC §103 over the Nguyen/Glass combination is respectfully traversed.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that amended claims 9-15 and 24-30 are in condition for allowance and notice to that effect is respectfully solicited. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, he is respectfully requested to contact Applicant's undersigned representative.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 

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